a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus.

8. (Amended) An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to said peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein,

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus.

15. (Amended) A method of carrying out data transfer by using a plurality of bus masters, comprising:

generating a request signal requesting a use of a data bus in units of the unit data bus in each of a plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

sending, in response to said request signal, a grant signal granting the use of said data bus in units of the unit data bus requested in unit data buses to said bus master in accordance with an availability of said data bus in units of the unit data bus;

and

occupying said data bus granted by said grant signal in units of the unit data bus, and carrying out data transfer by using the unit data buses thus occupied, wherein

the request signal and the grant signal indicate identification or number of the unit data bus divided from the data bus.

Please add new Claims 21-26 as follows:

21. (New) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein

the request signal and the grant signal are able to specify each of the unit data bus.

22. (New) An information processing system for carrying out data transfer by using a plurality of bus masters, comprising:

a peripheral apparatus;

a data bus connected to said peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, wherein

the request signal and the grant signal are able to specify each of the unit data bus.

23. (New) A method of carrying out data transfer by using a plurality of bus masters, comprising:

generating a request signal requesting a use of a data bus in units of the unit data bus in each of a plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

sending, in response to said request signal, a grant signal granting the use of said data bus in units of the unit data bus requested in unit data buses to said bus master in accordance with an availability of said data bus in units of the unit data bus; and

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occupying said data bus granted by said grant signal in units of the unit data bus, and carrying out data transfer by using the unit data buses thus occupied, wherein

the request signal and the grand signal are able to specify each of the unit data bus.

24. (New) A data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

a data bus connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, whereby

data in a memory and a register storing bus arbitration information is accessed concurrently through the unit data bus.

25. (New) An information processing system for carrying out data transfer by using a plurality of bus master, comprising:

a peripheral apparatus;

a data bus connected to said peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

a plurality of bus masters configured to send a request signal requesting a use of said data bus in units of the unit data bus, and using said data bus in unit data buses requested when a request by means of said request signal is granted; and

a bus controller configured to split-control said data bus in unit data buses for said plurality of bus masters by giving a grant signal which grants the use of said data bus in units of the unit data bus requested in unit data buses to said bus masters in accordance with an availability of said data bus in units of the unit data bus, whereby

data in a memory and a register storing bus arbitration information is accessed concurrently through the unit data bus.

26. (New) A method of carrying out data transfer by using a plurality of bus masters, comprising:

generating a request signal requesting a use of a data bus in units of the unit data bus in each of a plurality of bus masters and sending said each request signal to a bus controller, said data bus being connected to a peripheral apparatus and including a plurality of unit data buses, into which the data bus is divided and through each of which data is transferred concurrently;

sending, in response to said request signal, a grant signal granting the use of said data bus in units of the unit data bus requested in unit data buses to said bus master in accordance with an availability of said data bus in units of the unit data bus; and

occupying said data bus granted by said grant signal in units of the unit data bus, and carrying out data transfer by using the unit data buses thus occupied, whereby

data in a memory and a register storing bus arbitration information is accessed concurrently through the unit data bus.

REMARKS

Favorable reconsideration of this Application as presently amended and in light of the following discussion is respectfully requested.

After entry of the foregoing amendment, Claims 1-26 remain pending in the present application. Claims 1, 8 and 15 have been amended. Claims 21-26 have been newly added. Support for the amendment of Claims 1, 8 and 15 can be found at least on page 8, line 34 to page 9, line 3 of the Applicant's specification. Likewise, support for new Claims 21-26 may be found on page 8, lines 14-17; Figs. 4-5. No new matter has been added.

By way of summary, the Official Action presents the following issue: Claims 1-20 are rejected under 35 U.S.C. § 103 as being anticipated by Kato et al. (U.S. Patent No. 6,070,205, hereinafter Kato).

REJECTION UNDER 35 U.S.C. § 102

The Official Action has rejected Claims 1-20 as being unpatentable over Kato. The Official Action states that Kato discloses all the Applicant's claim limitations. Applicant respectfully traverses the rejection.

Amended Claim 1 recites, *inter alia*, a data transfer control circuit including: